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Implementation of Full-Bridge Single-Stage Converter with Reduced Auxiliary Components

G. Devanatha Reddy[1], P. R. Muralimohan[2]
[1]PG Student (PE&ED) Department of Electrical & Electronics Engineering S.V.C.E.T., Chittoor
[2]Associate Professor Department of Electrical & Electronics Engineering S.V.C.E.T., Chittoor

ABSTRACT
The inclusion of a few additional diodes and passive elements in the high-frequency full-bridge ac–dc converter with galvanic isolation permits one to achieve sinusoidal input-current wave shaping and output-voltage regulation simultaneously without adding any auxiliary transistors. Recently, this procedure, together with an appropriate control process, has been used to obtain low-cost high-efficiency single-stage converters. In an attempt to improve the performance of such converters, this paper introduces three new single-stage full-bridge ac–dc topologies with some optimized characteristics and compares them with the ones of the existing full-bridge single-stage topologies. The approach used consists in the definition of the operating principles identifying the boost function for each topology, their operating limits, and the dependence between the two involved conversion processes. Experimental results for each topology were obtained in 500-W modular voltage disturbances that result from the input-current wave-shaping process.

Index Terms: Full-bridge converters, input-current shaping, low-distortion input current, single-stage power-factor correctors.

I. INTRODUCTION

In modern switch mode power supplies (SMPSs) with galvanic isolation, the capacity to perform power factor correction (PFC) is a frequent characteristic, in compliance with the standard IEC-1000-3-2. This requirement is normally achieved with an additional input converter, typically a bridge rectifier, followed by a boost converter .For high power levels, the association of this input converter with the full-bridge isolated dc–dc converter results in a two stages converter with the inherent characteristics such as high cost and the necessity of having very high efficiency in each stage.

Recently, new PFC bridgeless promising solutions, mainly intent to replace the input rectifier and the boost converter, have emerged. These techniques are permitted to obtain good input current wave shaping with lower harmonic distortion and efficiency higher than the ones presented. However, to perform also high-frequency isolation and output dc voltage regulation, these topologies still need the presence of another converter (an isolated dc–dc converter). Thus, the overall system will result in a high-cost two-stage converter, gaining only an increase in the efficiency, when compared with the topologies resented. Consequently, these topologies are not suited for the application focused in this paper, which is based in one-stage converter.

Considering the constant interest of the industry in reducing the cost and the increase of efficiency of the SMPS, while maintaining the PFC function, several topologies of isolated ac/dc single-stage SMPS have been proposed, based on the forward and fly back dc–dc converters for low-power applications. However, in the case of high-power applications, the voltage and current ratings of the power transistor and diodes increase considerably, thereby rising the cost of these solutions to values that can be even higher than those observed in the two-stage topologies. In view of the power limitation of these topologies, single-stage isolated full-bridge topologies with PFC function have been proposed recently.

These topologies can perform input current wave shaping and output voltage control, simultaneously, without using any additional transistors. However, these topologies are not optimized in terms of additional components and current distribution in the bridge transistors. For example, in the topologies presented, only two parallel input boost converters are provided using the low-side transistors, which leads to asymmetrical current distribution in the bridge transistors causing, in these transistors, a high current stress. An input bridge rectifier is also needed for these topologies. For the topologies proposed, only one input inductor is used, but this inductor and the two low-side transistors have to support the maximum input current. On the other hand, the topology presented uses two inductors for half of the maximum input current, which means that, each low-side boost transistor needs only to support half of the maximum input current, thereby reducing the current stress in these transistors. However, the topology uses

six additional diodes, thus increasing the cost and reducing the efficiency.

In an attempt to solve the referred problems, this project presents an optimized and improved single-stage full-bridge ac/dc converter, where the input bridge rectifier was replaced by two rectifier diodes.

This fact obviously allows, by itself, a slight improvement in the converter efficiency. In addition, it also guarantees the improvement of the converter by performing four input boosts, to accomplish the PFC function, instead of two as it is common in other existing topologies. This way, the operation of the proposed topology will result symmetric, with all the inherent advantages in terms of current and voltage switches' stress reduction. Full analysis and design criteria are completely described in this project.

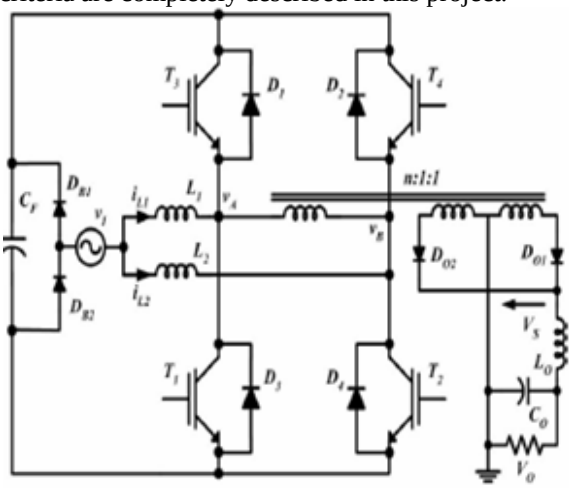

Fig.1. High-efficiency full-bridge single stage topology

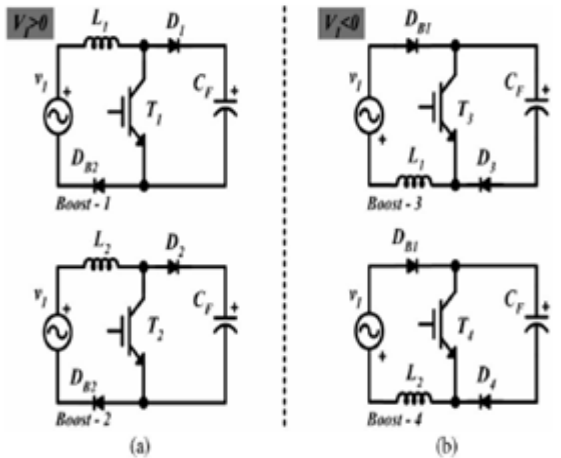

Fig.2. Four boost converters provided by the topology. (a) low-side transistors and (b) high-side transistors.

The diverse existing topologies are compared in terms of efficiency, input- current total harmonic distortion (THD), and output-voltage ripple. To achieve an accurate comparison, the specifications in terms of power and output and input voltages were the same in all the topologies, with an exception for topology I, as shown in Fig. 1 (which was experimented for half of the input voltage due to limitations inherent to this topology). The output-voltage and input-current controllers were also common for all topologies.

II. OPERATING PRINCIPLES AND TOPOLOGY ANALYSIS

Two auxiliary diodes *DB*1 and *DB*2 are used instead to guarantee the operation of the boost converters provided. The topology provides four boost converters: two boosts realized by the low-side transistors (*T*1 and *T*2) when $vI > 0$ and another two provided by the high-side transistors (*T*3 and *T*4) when $vI < 0$

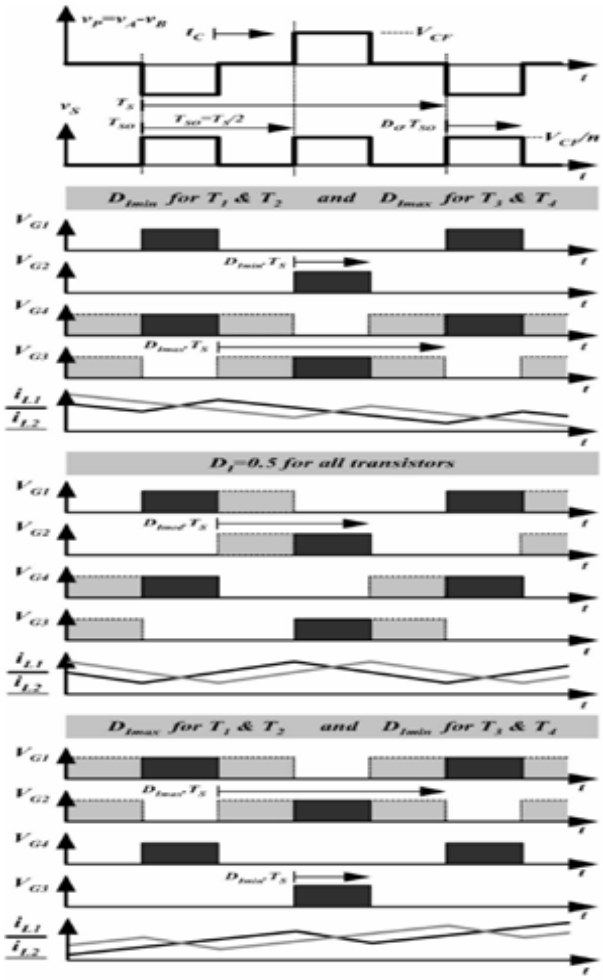

Fig.3: Transformer primary voltage V_p rectified

The control of the input current is achieved by the same way as in topology I, i.e., by the selection of the states S00 or S11 during the time intervals where $vP = 0$. Fig. 2 shows the most relevant waveforms that allow the identification of the two duty ratios *DI* and *DO*. The evolution of the current in the input inductance *L* is also presented. In this figure, the

particular case when $vI < 0$ was considered. For the present topology, the input-current switching frequency is *FS*.

As what occurs in topology I, the adoption between the two states S00 or S11 results in a discrete variation of the input-duty ratio

$$D_{Imin} = DO/2 \quad (1)$$

$$D_{Imed}=0.5 \quad (2)$$

$$D_{Imax} = 1 - DO/2 \quad (3)$$

The maximum control angle αmax is the first parameter to be defined. Considering the adopted value for αmax, the maximum output duty ratio is defined according to the restriction.

The value of voltage *V*CF is then established, considering the defined values of *DO* and αmax . For topologies II–VI, the adoption of the *DO* and *V*CF values results in a new value of αmax

$$\alpha\max = \sin^{-1}(VCF/VImin \cdot DO/2) \quad (4)$$

Considering the operation in CCM of the output filter, the output duty ratio is constant. Therefore, the minimum input duty ratio *D*Imin imposes a minimum input power *P*Imin(CCM). Neglecting the converter losses, this minimum input power must be absorbed by the load to guarantee the *V*CF voltage control. This problem can be surpassed, considering the operation of the output filter in DCM which reduces *DO* and *D*Imin with low loads and consequently decreases the minimum input power. To avoid the situation wherein the output filter operates in DCM for large loads, the input inductances of the topologies are designed considering a minimum input power at which the output filter operates in CCM. The minimum input power is obtained by excess, considering that the boost converters generate a sinusoidal input current that has an amplitude equal to the maximum value expressed by (11)–(14) [the worst case was considered: *VI* = *V*Imax and *V*CF = *V*CFmin defined from condition]

The design of the capacitor *CF* is obtained according to the capacitor voltage ripple ΔVCF, which is normally < 5%, considering the maximum output power and the expected efficiency η to guarantee the *V*CF control, it is necessary that the output power boundary *P*OB will be greater than *P*Imin(CCM) ·

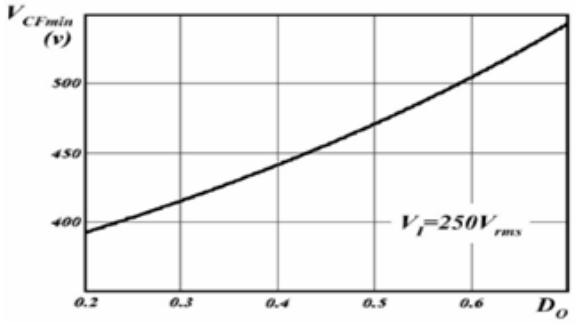

Fig.4: $V_{CF\ min}$ as function of DO for an Input voltage Vrms=250v

III. MINIMUM INPUT POWER

Considering the operation in CCM of the output filter, the output duty ratio is constant. Therefore, the minimum input duty ratio *D*Imin imposes a minimum input power *P*Imin(CCM).

Neglecting the converter losses, this minimum input power must be absorbed by the load to guarantee the *V*CF voltage control. This problem can be surpassed, considering the operation of the output filter in DCM which reduces *DO* and *D*Imin with low loads and consequently decreases the minimum input power. To avoid the situation wherein the output filter operates in DCM for large loads, the input inductances of the topologies are designed considering a minimum input power at which the output filter operates in CCM. The minimum input power is obtained by excess, considering that the boost converters generate a sinusoidal input current that has an amplitude equal to the maximum value expressed by (11)–(14).

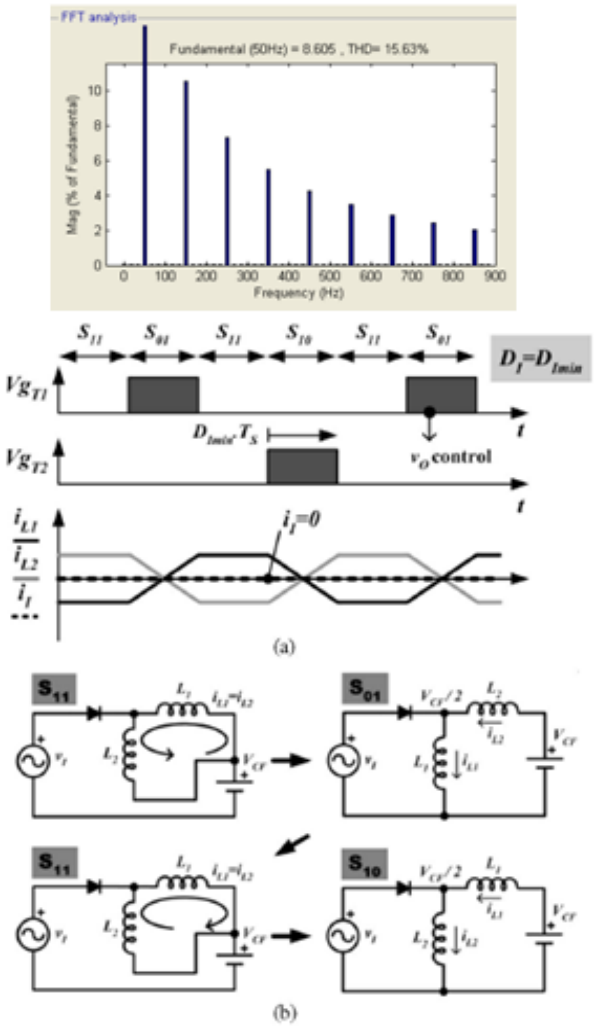

Fig.5:Constant operation of two low side boosts with $D_I=D_{Imin}$ (a).Gate signals of T1, T2 and inductor currents (b) Equivalent circuit used to present the converter states

For the input-current control, a hysteretic comparator is used to compare the reference current with the input current *iI* and select the appropriate state S00 or S11 during the intervals where *vP* = 0to achieve the sinusoidal input-current wave shaping. A
low-cost analog multiplier, namely, AD633, is used to define the current reference which is proportional to the integration of the error in the *V*CF voltage capacitor. For the output-voltage regulator, a voltage-mode modulator is used. An additional logic circuit generates the gate signals. In the experimental results, a hysteretic current of 0.3 A was considered. A linear resistive sensor and a differential amplifier can also be used, replacing the Hall effect sensor.

IV. SIMULATION RESULTS

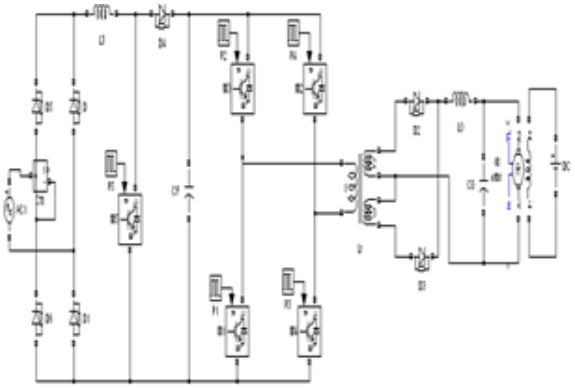

Fig.6: Conventional two stage topology

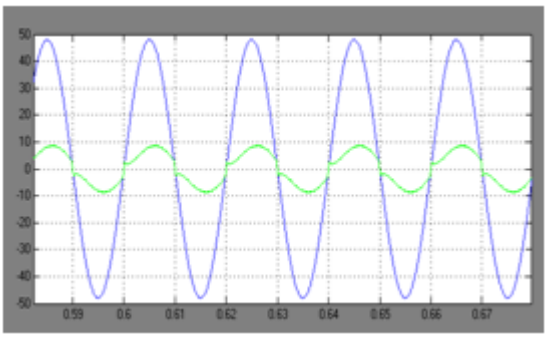

Fig.7: input voltage and currents

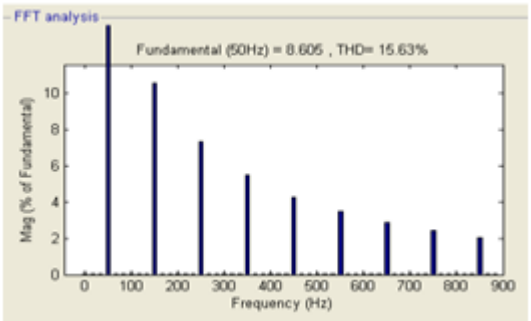

Fig.8: THD for the conventional topology

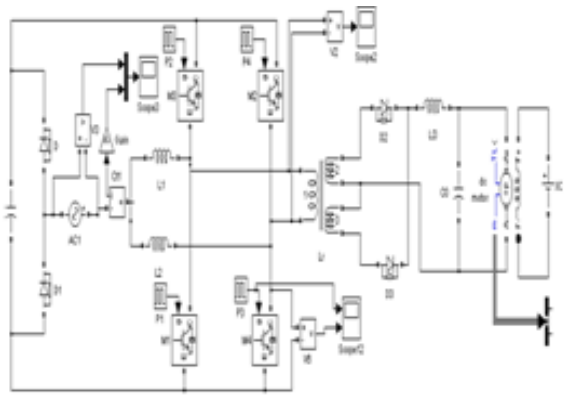

Fig.9: Proposed single stage topology

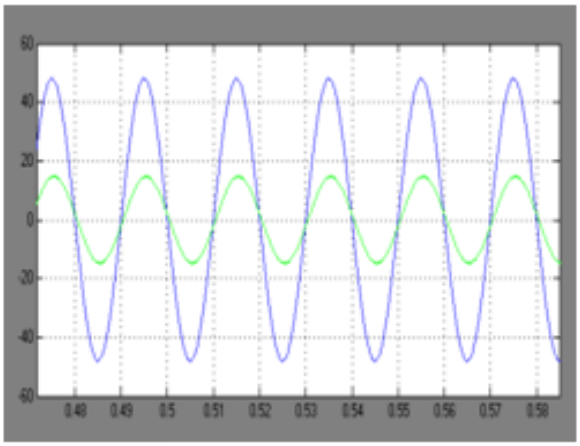

Fig.10: input voltage and currents

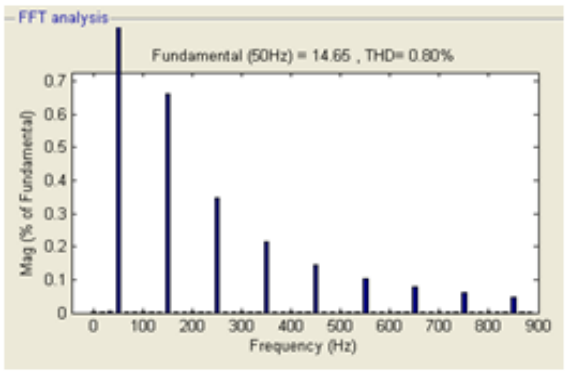

Fig.11: THD for the proposed topology

V. CONCLUSION

In this Work, The simulink/Matlab based Conventional and Proposed circuits has been Developed and described a comparison of existing Conventional single stage full-bridge converter and introducing proposed single stage full-bridge converter to improve some drawbacks of existing ones. The most important characteristics were identified and compared. According to the comparison analysis Obtained, it is possible to conclude that, the number of stages in the existing circuit was reduced to single stage. The additional

components(Boost converters, induction coils, etc..,) was eliminated.The Device rating Was More Utilised By the Proposed Circuit.

REFERENCES

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "*A review of single-phase improved power quality ac–dc converters*," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.

[2] E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "*Buck-boost-type unity power factor rectifier with extended voltage conversion ratio*," *IEEE Trans. Power Electron.*, vol. 55, no. 3, pp. 1123–1132, Mar. 2008.

[3] M.M. Jovanovi and Y. Jang, "*State-of-the-art, single-phase, active powerfactor-correction techniques for high-power applications—An overview*," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 701–708, Jun. 2005.

[4] L. Huber, Y. Jang, and M. M. Jovanovi, "*Performance evaluation of bridgeless PFC boost rectifiers*," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.

[5] Y. Jang and M. M. Jovanovi, "*A bridgeless PFC boost rectifier with optimized magnetic utilization," IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 85–93, Jan. 2009.

[6] W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo, "*A novel bridgeless buck–boost PFC converter*," in *Proc. IEEE Power Electron. Spec. Conf.*,2008, pp. 1304–1308.

[7] W.-Y. Choi, J.-M. Kwon, and B.-H. Kwon, "*Bridgeless dual-boost rectifier with reduced diode reverse-recovery problems for power-factor correction*," *IET Power Electron.*, vol. 1, no. 2, pp. 194–202, Jun. 2008.

[8] R. Redl, L. Balogh, and N. O. Sokal, "*A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage*," in *Proc. IEEE Power Electron. Spec. Conf.*, 1994, pp. 1137–1144.

[9] R. Redl and L. Balogh, "*Design considerations for single-stage isolated power-factor-corrected power supplies with fast regulation of the output voltage*," in *Proc. IEEE Appl. Power Electron. Conf.*, 1995, pp. 454–458.

[10] C. Qiao and K. M. Smedley, "*A topology survey of single-stage power factor corrector with a boost type input-current-shaper*," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 360–368, May 2001.

[11] O. Garcia, J. A. Cobos, P. Alou, R. Prieto, and J. Uceda, "*A simple singleswitch single-stage ac/dc converter with fast output voltage regulation*," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 163–171, Mar. 2002.

[12] Q. Zhao, F.C. Lee, and F.-S. Tsai, "*Voltage and current stress reduction in single-stage power factor correction ac/dc converters with bulk capacitor voltage feedback*," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 477– 484, Jul. 2002.

[13] S. Luo,W. Qiu,W.Wu, and I. Batarseh, "*Flyboost power factor correction cell and a new family of single-stage ac/dc converters*," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 25–34, Jan. 2005.

[14] H.-F. Liu and L.-K. Chang, "*Flexible and low cost design for a flyback ac/dc converter with harmonic current correction*," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 17–24, Jan. 2005.

[15] J.-Y. Lee, "*Single-stage ac/dc converter with input-current dead-zone control for wide input voltage ranges," IEEE Trans. Power Electron.*, vol. 54, no. 2, pp. 724–732, Apr. 2007.

[16] D. D.-C. Lu, H. H.-C. Iu, and V. Pjevalica, "*A single-stage ac/dc converter with high power factor, regulated bus voltage, and output voltage*," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 218–228, Jan. 2008.

[17] A. Lázaro, A. Barrado, M. Sanz, V. Salas, and E. Olías, "*New power factor correction ac–dc converter with reduced storage capacitor voltage," IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 384–397, Feb. 2008.

[18] J. Zhang, M. M. Jovanovic, and F. C. Lee, "*Comparison between CCM single-stage and two-stage boost PFC converters*," in *Proc. Appl. Power Electron. Conf.*, 1999, vol. 1, pp. 335–341.

[19] M. Qiu, G. Moschopoulos, H. Pinheiro, and P. Jain, "*Analysis and design of a single stage power factor corrected full-bridge converter,"* in *Proc. IEEE Appl. Power Electron. Conf.*, 1999, pp. 119–125.

[20] S. Li and G. Moschopoulos, "*A simple AC–DC PWM full-bridge converter with auxiliary transformer winding*," in *Proc. IEEE INTELEC*, 2003, pp. 216–223.

[21] G. Moschopoulos and P. Jain, "*Single-phase single-stage power-factorcorrected converter topologies*," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 23–35, Feb. 2005.

[22] L. Rosseto and S. Buso, "*Single-phase AC/DC integrated PWM converter*," in *Proc. INTELEC*, 2000, pp. 411–418.
[23] L. Rosseto and S. Buso, "*Digitally-controlled single-phase AC/DC integrated PWM converter*," in *Conf. Rec. IEEE IAS Annu. Meeting*, Oct., pp. 2159–2166.
[24] L. Rosseto and S. Buso, "*Digitally-controlled single-phase single-stage ac/dc PWM converter*," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 326–333, Jan. 2003.
[25] V. Anunciada and R. D. Monteiro, "*Single stage full-bridge converter with power factor correction*," in *Proc. IEEE Power Electron. Spec. Conf.*, 2001, pp. 1566–1570.
[26] V. Anunciada and H. Ribeiro, "*Single stage AC/DC converter with input power factor correction*," in *Proc. IEEE IECON*, 2003, pp. 2933–2938.
[27] V. Anunciada and H. Ribeiro, "*Single stage AC/DC converter with input power factor correction*," in *Proc. PEDS*, 2003, pp. 1480–1485.
[28] V. Anunciada and B. Borges, "*Power factor correction in single phase AC–DC conversion: Control circuits for performance optimization*," in *Proc. IEEE Power Electron. Spec. Conf.*, 2004, pp. 3775–3779.